REMARKS

Claims 2-13 and 15-22 are pending in this application. By this amendment, Applicant cancels claims 1 and 14 and amends claims 2-10, 12, 13 and 15-22.

The Examiner's indication of claims 6-8, 13 and 20 as being allowable if rewritten in independent form and including all of the features of the base claim and any intervening claims is appreciated.

Claims 9 and 21 were rejected under 35 U.S.C. § 112, second paragraph, for allegedly being indefinite. Particularly, the Examiner alleges that "the term 'LC π type' is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention". Applicant respectfully disagrees.

The term "π type low pass filter" refers to a conventional filter configuration that is notoriously well-known in the art. Applicant provides herewith a copy of two pages from the book, "Illustrated Guide to Basic Electronics With Useful Projects and Experiments" by John Steiner, which clearly describes and illustrates a π type filter circuit.

Accordingly, Applicant respectfully submits that the term "LC π type" is a conventionally well-known term in the art, and thus that claims 9 and 21 positively and definitely recite the claimed invention. Accordingly, Applicant respectfully requests reconsideration and withdrawal of this rejection.

Claims 1-3, 5, 10, 12, 14-17, 19 and 22 were rejected under 35 U.S.C. § 102(b) as being anticipated by Mandai et al. (U.S. 5,436,601). And, claims 4 and 18 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Mandai et al.

Applicant has amended allowable claims 6, 7, 8, 13 to include all of the features of claim 1, and further has amended allowable claim 20 to include all of the features of claim 14. Accordingly, Applicant respectfully submits that claims 6, 7, 8, 13 and 20 are allowable as indicated by the Examiner.

In view of the foregoing amendments and remarks, Applicant respectfully submits that Claims 6, 7, 8, 13 and 20 are allowable over the prior art for the reasons described

above. Claims 2-5, 9-12, 15-19, 21 and 22 are dependent upon claims 8 and 20, and are therefore allowable for at least the reasons that claims 8 and 20 are allowable.

In view of the foregoing Remarks, Applicant respectfully submits that this Application is in condition for allowance. Favorable consideration and prompt allowance are respectfully solicited.

The Commissioner is authorized to charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1353.

Respectfully submitted,

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VERSION WITH MARKINGS SHOWING CHANGES MADE

2. The delay line according to claim [1] 8, wherein the at least three inductors are defined by a plurality of coil conductor patterns arranged on the same plane of the insulating layers of the laminated body.

3. The delay line according to claim [1] 8, wherein each of the at least three inductors has a coil axis that is substantially parallel with a laminating direction of the insulating layers of the laminated body, and winding directions of adjacent ones of the at least three inductors are opposite to each other.

4. The delay line according to claim [1] 8, wherein the insulating layers are made of a dielectric ceramic material having a relative dielectric constant of about 15 or less.

5. The delay line according to claim [1] 8, wherein one of the plurality of capacitors is connected to an end of at least one of the at least three inductors, and another of the plurality of capacitors is connected to another end of said at least one of the at least three inductors, are located at different positions in a laminating direction of the insulating layers.

6. [The] A delay line [according to claim 2,] comprising:

a coil divided into at least three inductors; and

a laminated body including a plurality of insulating layers and at least three stages of low pass filters including said at least three inductors and a plurality of capacitors; wherein

a ratio of a vertical dimension to a lateral dimension of each of the coil conductor patterns is approximately 1.

7. [The] A delay line [according to claim 1,] comprising:

a coil divided into at least three inductors; and

a laminated body including a plurality of insulating layers and at least three

stages of low pass filters including said at least three inductors and a plurality of capacitors; wherein

one end of a first of the at least three inductors of a k stage in the low pass filter and one end of a second of the at least three inductors of a k+1 stage adjacent thereto in the low pass filter are electrically connected to each other on an upper layer of the laminated body, and the second end of the another of the at least three inductors of the k+1 stage in the low pass filter and one end of a third of the at least three inductors of a k+2 stage adjacent thereto in the low pass filter are electrically connected to each other on a lower layer of the laminated body.

8. [The] A delay line [according to claim 1,] comprising:

a coil divided into at least three inductors; and

a laminated body including a plurality of insulating layers and at least three stages of low pass filters including said at least three inductors and a plurality of capacitors; wherein

the coil is divided into at least four inductors.

9. The delay line according to claim [1] 8, wherein the low pass filters are LC π type low pass filters.

10. The delay line according to claim 2, wherein the insulating [sheets] layers have a plurality of via holes for connecting the coil conductor patterns that define the at least three inductors.

12. The delay line according to claim [1] 8, wherein the number of the plurality of capacitors is greater than the number of the inductors.

13. [The] A delay line [according tc claim 1,] comprising:

a coil divided into at least three inductors; and

a laminated body including a plurality of insulating layers and at least three stages of low pass filters including said at least three inductors and a plurality of capacitors; wherein

the insulating layers include magnetic material.

15. The monolithic circuit array according to claim [14] 20, wherein at least three inductors and at least four capacitors are included in the at least three stages of low pass filters.

16. The monolithic circuit array according to claim [14] 20, wherein at least four stages of low pass filters are provided in the monolithic laminated body, and at least four inductors and at least five capacitors are included in the at least four stages of low pass filters.

17. The monolithic circuit array according to claim [14] 20, wherein the inductors are defined by a plurality of coil conductor patterns arranged on the same plane of the insulating layers of the laminated body.

18. The monolithic circuit array according to claim [14] 20, wherein the insulating layers are made of a dielectric ceramic material having a relative dielectric constant of about 15 or less.

19. The monolithic circuit array according to claim [14] 20, wherein one of the capacitors is connected to an end of at least one of the inductors, and another of the capacitors is connected to another end of said at least one of the inductors, and the one of the capacitors and the another of the capacitors are located at different positions in a laminating direction of the insulating layers.

20. [The] A monolithic circuit array [according to claim 17,] including a delay line comprising:

a coil divided into at least three inductors; and

a plurality of insulating layers stacked on each other to define a monolithic laminated body, the laminated body including at least three stages of low pass filters defined by lumped constant inductors and capacitors; wherein

a ratio of a vertical dimension to a lateral dimension of each of the coil conductor patterns is approximately 1.

21. The monolithic circuit array according to claim [14] 20, wherein the low pass filters are LC π type low pass filters.

22. The monolithic circuit array according to claim [14] 20, wherein the number of the plurality of capacitors is greater than the number of the inductors.